REMARKS

Claims 1-5, 7-8, 10-18 and 35-54 are pending in the current application. Claims 1, 12 and 14 are independent claims.

35 U.S.C. § 112, 1st Paragraph, Written Description

Claims 1, 12 and 14 are rejected under 35 U.S.C. § 112, first paragraph, for allegedly failing to comply with the written description requirement. Applicant respectfully traverses this rejection.

The Examiner alleges that the limitation "wherein the on-chip memory is selectably filled with data from an external memory independent of cache accesses of the cache memory" is not supported by the Specification as originally filed because the original Specification merely describes filling the on-chip memory with external data in advance of an eventual cache access. Applicant respectfully disagrees with the Examiner's interpretation of this claim language.

Applicant directs the Examiner to Figure 3 of the application, which shows on-chip memory 350 connected to external main memory 360 via DME controller 352 and separately connected to cache memory 340 via DMA controller 344 and/or cache controller 342. The connection between the on-chip memory 350 and the external main memory 360 is independent of the cache memory 340 in the sense that the cache memory 340 need not be involved in an interaction between the on-chip memory 350 and external main memory 360 (e.g., see [0036]).

As noted by the Examiner, one potential reason why a user would transfer data to the on-chip memory "is that the user/programmer can arrange to have the instructions and data required by processor core 330 to be present in on-chip memory 350 well in advance of when they are actually needed by the processor core" (See [0037]). However, the actual user-controlled

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transfer of data to the on-chip memory 350 does not depend on an eventual cache access of the transferred data ever taking place. In other words, this transfer of data is not dependent on a cache-access. By contrast, if data were only loaded into the on-chip memory *in response* to a cache hit or miss, then the loading of the data would be dependent on the cache access. The fact that the transferred data may potentially aid a future scenario where a cache miss for the transferred data occurs does not make the earlier transfer of the data dependent on the cache access.

Further, the Examiner's reference to on-chip memory provided with data "in advance" of when it is needed is merely listed as an example of one advantage of an embodiment of he invention (e.g., see [0037]). Nothing in the Specification says the eventual cache access *must* occur, or that the user will transfer the data only if it knows the eventual cache access will occur. For example, paragraph [0047] discusses how the on-chip memory 450 becomes the worst-case scenario for data retrieval, which means the on-chip memory 450 may be transferred data that is expected to be accessed, but is not actually accessed, unless the user transfers data with perfect foresight.

In any case, Applicant submits that an earlier transfer of data to an on-chip memory is not dependent upon a processor looking for that data in a cache at some future point in time, and as such the claim language of "wherein the on-chip memory is selectably filled with data from an external memory independent of cache accesses of the cache memory" is supported by the Specification as originally filed.

Applicant respectfully requests that the Examiner withdraw this rejection.

35 U.S.C. § 103(a) Volpe in view of Boyle

Claims 1-5, 7, 10-13, 35, 38-40, 43-46, 49 and 52-54 were rejected under 35 U.S.C. §

103 (a) as allegedly being unpatentable over Volpe (U.S. Patent No. 6,895,475) in view of Boyle

(U.S. Patent No. 7,194,576). Applicant respectfully traverses this art grounds of rejection.

As an initial matter, Applicant notes that the Patent No. listed for Boyle is incorrectly

listed on page 3 of the 5/2/2008 final Office Action. Applicant's representative Daniel Podhajny

(Reg. No. 57,687) called Examiner Song on 6/11/2008, and Examiner Song indicated that the

correct Patent No. for Boyle was 7,194,576.

Volpe is directed to a prefetch buffer method and apparatus. The Examiner reads the

claimed "processor core" upon core processor 10 of Figure 1 of Volpe, the claimed "cache

memory" upon L1 data memory of Figure 1 of Volpe, and the claimed "on-chip memory" upon

prefetch buffer 260 of Figure 3 of Volpe (See Pages 3-4 of the Office Action). Applicant agrees

with the Examiner in that the prefetch buffer 260 fails to disclose "that the [prefetch buffer 260]

is selectably filled with data from an external memory independent of cache access of cache

memory under user control" (See Page 4 of the Office Action). The Examiner alleges that Boyle

discloses this particular deficiency of Volpe.

The Examiner primarily cites to Figure 3 and steps 316-320 of Boyle as disclosing

filling, with data, an on-chip memory independent of a cache access. Applicant respectfully

disagrees, and will now explain how Boyle's process of Figure 3 is entirely dependent upon a

cache access.

Referring to Figure 3 of Boyle, in step 310, a cache controller 204 receives a request for

either (i) an instruction code or (ii) non-instruction data (See Figure 3 and Column 3, lines 19-25

of Boyle). Next, in step 312, the cache controller 204 checks a cache memory 207 to determine

whether the requested data is already available (See Figure 3 and Column 3, lines 34-42 of

Boyle). If the data (i.e., either the instruction code or non-instruction data) is available, the data

cache controller 204 simply loads and transfers the requested data from the cache memory 207 to

the requesting entity (See Figure 3, step 312, and Column 3, lines 34-42 of Boyle). If the

requested data is not readily available, the cache controller 204 determines whether the data

request is for non-instruction data (step 314 of Figure 3, Boyle). If the data request is for non-

instruction data, the cache controller 204 fetches the non-instruction data from a remote memory

without actually updating the cache memory 207 to include the fetched data (steps 316, 318 of

Figure 3, Boyle).

The reason for Boyle's cache-bypass at step 318 of Figure 3 is that instruction codes are

more likely to repeat than non-instruction data. Thus, it is better to reserve cache-space for

instruction codes and only retrieve non-instruction data when needed because the data will be

requested less frequently, and as such a cache miss resultant in latency is not such a big deal.

Still, whether or not requested data is ever actually stored in the cache is largely irrelevant. In

Boyle, the cache is accessed in steps 310/312 where the cache controller 204 determines whether

the requested data is actually in the cache memory 207. Clearly, this determination could not be

made if the cache memory 207 were not accessed to determine a cache hit or miss. If there is a

cache-hit, the data is simply provided from the cache (step 312). If there is a cache miss, then

instruction code is fetched and stored in the cache (implicit within Figure 3), whereas non-

instruction data is simply fetched (step 318). Each operation in Figure 3 is dependent upon first

evaluating whether the requested data is actually in the cache, and this means the entire process

of Figure 3 is dependent upon a cache access for the requested data. The mere fact that the cache

is not necessarily accessed again at step 318 (although for instruction codes, it would be) does

not negate the dependency of Figure 3 of Boyle upon the initial cache access, because steps 314-320 only occur if there is determined to be a cache miss.

Accordingly, Applicant respectfully submits that Volpe in view of Boyle cannot disclose or suggest "wherein the on-chip memory is selectably filled with data from an external memory independent of cache accesses of the cache memory under user control" as recited in independent claim 1 and similarly recited in independent claim 12.

As such, claims 2-5, 10-11, 13, 35, 38-40, 43-46, 49 and 52-54, dependent upon independent claims 1 and 12, respectively, are likewise allowable over Volpe in view of Boyle at least for the reasons given above with respect to independent claims 1 and 12.

Applicant respectfully requests that the Examiner withdraw this art grounds of rejection.

35 U.S.C. § 103(a) Volpe in view of Boyle in further view of Ramchandran

Claim 8 is rejected under 35 U.S.C. § 103 (a) as allegedly being unpatentable over Volpe (U.S. Patent No. 6,895,475) in view of Boyle (U.S. Patent No. 7,194,576) in further view of Ramchandran (U.S. Publication No. 2004/0093479). Applicant respectfully traverses this art grounds of rejection.

Ramchandran is directed to a cache for instruction set architecture using indexes to achieve compression. A review of Ramchandran indicates that Ramchandran cannot cure the suggestion and disclosure deficiencies of Volpe in view of Boyle as discussed above with respect to independent claim 1.

As such, claim 8, dependent upon independent claim 1, is likewise allowable over Volpe in view of Boyle in further view of Ramchandran at least for the reasons given above with respect to independent claim 1.

Applicant respectfully requests that the Examiner withdraw this art grounds of rejection.

35 U.S.C. § 103(a) Volpe in view of Boyle in further view of Kreitzer

Claims 41-42 and 50-51 were rejected under 35 U.S.C. § 103 (a) as allegedly being unpatentable over Volpe (U.S. Patent No. 6,895,475) in view of Boyle (U.S. Patent No. 7,194,576) in further view of Kreitzer (U.S. Publication No. 2005/0025315). Applicant respectfully traverses this art grounds of rejection.

Kreitzer is directed to a method and apparatus for secure communications among portable communication devices. A review of Kreitzer indicates that Kreitzer cannot cure the suggestion and disclosure deficiencies of Volpe in view of Boyle as discussed above with respect to independent claims 1 and 12.

As such, claims 41-42 and 50-51, dependent upon independent claims 1 and 12, respectively, are likewise allowable over Volpe in view of Boyle in further view of Kreitzer at least for the reasons given above with respect to independent claim 1.

Applicant respectfully requests that the Examiner withdraw this art grounds of rejection.

35 U.S.C. § 103(a) Volpe in view of Boyle in further view of Wing

Claims 14-18 were rejected under 35 U.S.C. § 103 (a) as allegedly being unpatentable over Volpe (U.S. Patent No. 6,895,475) in view of Boyle (U.S. Patent No. 7,194,576) in further view of Wing (U.S. Patent No. 5,987,590). Applicant respectfully traverses this art grounds of rejection.

Initially, Applicant respectfully submits that Volpe in view of Boyle cannot disclose or suggest "wherein the on-chip memory is selectably filled with data from an external memory

independent of cache accesses of the cache memory under user control" (Emphasis added) as recited in independent claim 14, at least for the reasons set forth above with respect to independent claims 1 and 2. Further, Wing is directed to PC circuits, systems and methods. A review of Wing indicates that Wing cannot cure the suggestion and disclosure deficiencies of Volpe in view of Boyle as discussed above with respect to independent claim 14.

As such, claims 15-18, dependent upon independent 14, are likewise allowable over Volpe in view of Boyle in further view of Wing at least for the reasons given above with respect to independent claim 14.

Applicant respectfully requests that the Examiner withdraw this art grounds of rejection.

CONCLUSION

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is in condition for allowance. If the Examiner believes that any additional changes would place the application in better condition for allowance, the Examiner is invited to contact the undersigned attorney, at the telephone number listed below.

Deposit Account Authorization

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any fees or overpayments that may be due with this response to Deposit Account No. 17-0026.

Respectfully submitted,

Dated: July 7, 2008   /John Luigi Ciccozzi/
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